MGS2401Q64CF8R16

Technical Datasheet

MINDGROVE

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Contents

1 Product overview

Mindgrove Silicon's MGS2401 is a high performance microcontroller targeting the IoT and embedded domains. It offers optimized power consumption at a high clock frequency with a large number of I/Os and peripherals. Also included is a security complex that accelerates cryptographic algorithms and stores secure information such as cryptographic keys.

1.1 Features

- Compute core:
  - 1x Shakti C-Class 64 bit RISC-V core
  - 6-stage In-Order operation
  - RV64GC (RV64IMAFDC)
  - 16kB I-Cache
  - 16kB D-cache
  - 700 MHz clock frequency
- 128 kB on-chip SRAM (OCSRAM)
- 8 Mbit QSPI Flash
- 16 Mbit QSPI PSRAM
- Peripherals
  - 2xQSPI
    - Supports SDR Mode
    - XIP Mode
    - RAM Mode
    - Has Interrupt functionality
  - 2xSPI
    - Can be configured as Master/Slave
    - Data transfers upto 35Mbps
    - Compliant with JESD251C
    - Has Interrupt functionality
  - 1xI2C
    - Supports only Master mode
    - Standard Mode (upto 100 kHz)
    - Fast Mode (upto 400 kHz)
    - High Speed Mode (upto 1MHz)
    - Has Interrupt functionality
  - 5xUART
    - 2-bit Parity
    - 0-2 Stop Bits
    - Supports 5 to 8-bit characters
    - Has Interrupt functionality
  - 21xGPIO
    - Rated to work at 1MHz.
    - 7-GPIOs Multiplexed with PWMs
    - 4-GPIOs Multiplexed with UARTs
    - 3-GPIOs Multiplexed with SPIs
    - 3-GPIOs Multiplexed with JTAG
    - 1-GPIOs Multiplexed with GPTimer
  - 7xPWM
    - Counter Reset
    - Complementary Output
    - Rise/Fall Interrupt
    - Half Period Interrupt
  - 1xADC
    - 12-Bit Successive Approximation Register (SAR) ADC
    - 4 Channels
    - 5MSPS Conversion Rate
    - 8:1 Multiplexed Inputs
  - 1xGPTimer
  - 1xWatchdog Timer
  - 1xPLIC
  - 1xCLINT
  - 1xDMA
    - 8 independent channels.
- Security
  - Hardware Crypto Accelerators
    - AES
      - Supports 128, 192, 256 Bits
      - Supports CBC, CFB, OFB, CTR modes
    - RSA 2048
    - SHA 2 - 256
    - True Random Number Generator
  - On-chip secure memory
    - 4kB on-chip OTP memory
  - Secure Boot
- Operating voltage
  - Core: 0.9V
  - I/O: 1.8V
- Packages:
  - 64-Pin QFN Package

2 Ordering Information

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact MG sales office.

2.1 Ordering Code Format

```
MG{SocName}-{PackageDetails}{TemperatureGrade}{CoPackageDetails}-{PackageType}
      |         |                |                 |              |
      |         |                |                 |              └─> [Package Type]
      |         |                |                 └────────────────> [Co-Package Details]
      |         |                └──────────────────────────────────> [Temperature Grade]
      |         └───────────────────────────────────────────────────> [Package Details]
      └─────────────────────────────────────────────────────────────> [SoC Name]
```

2.1.1 Code Breakdown

- **Device Family:** MGS = MindGrove silicon SecureIoT
- **Package Details:**
  - **B144** – BGA 144 pins
  - **Q64** – QFN 64 pins
- **Co-Package Details:**
  - **F8R8** – Flash: 8 Mbit, PSRAM: 8 Mbit
  - **F8R16** – Flash: 8 Mbit, PSRAM: 16 Mbit
  - **F16** – Flash: 16 Mbit
  - **F02** – Flash: 256 Kbit
- **Temperature Grade:**
  - **C** – Consumer (0 °C to +85 °C)
- **Package Type:**
  - **T** – Tape
  - **R** – Reel
  - **B** – Tray

2.2 Example Ordering Code

`MGS2401-B144C-B`

`MGS2401-Q64C-F8R16-B`

3 Block diagram

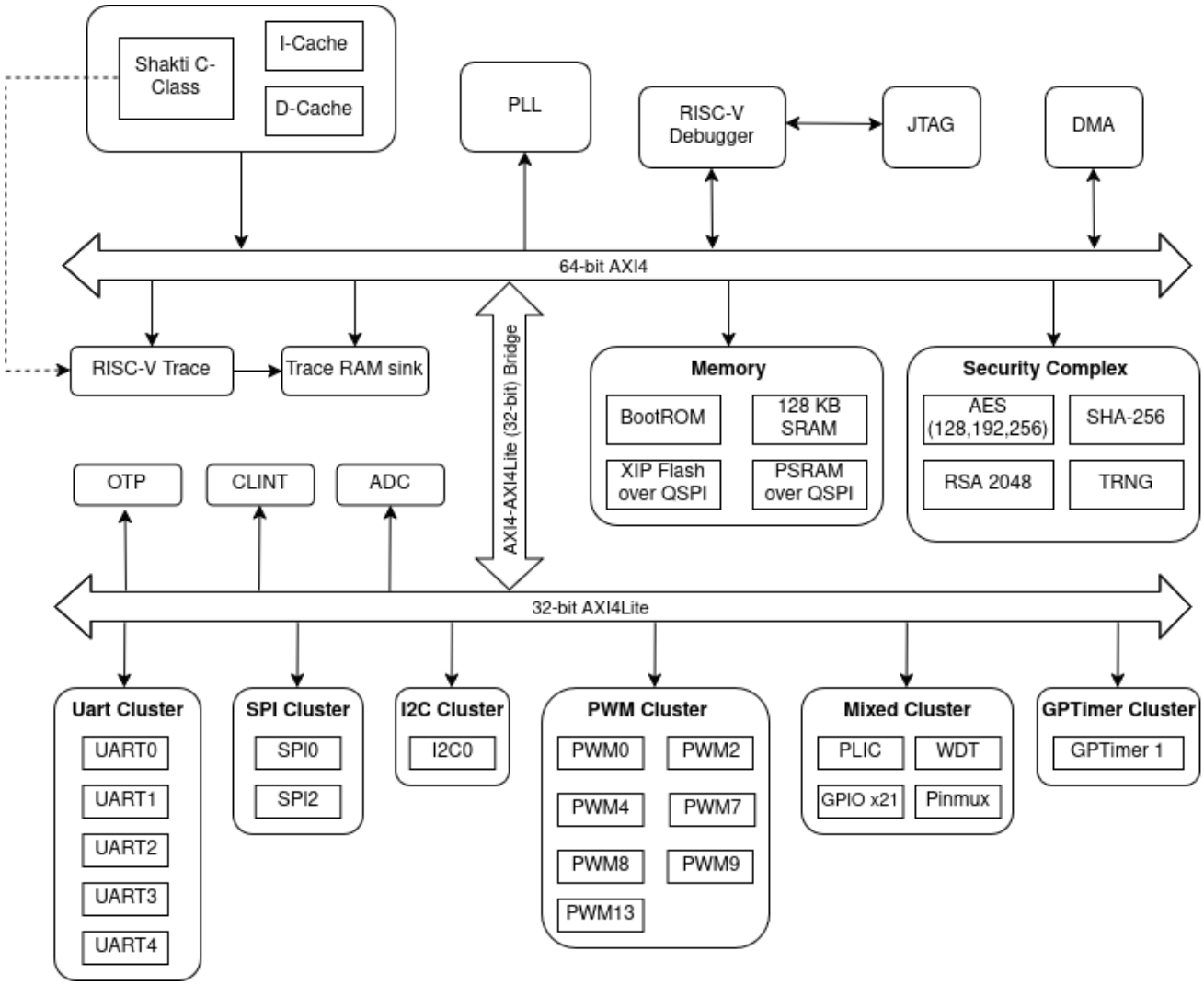

Figure 1: MGS2401 QFN Block Diagram

4 Pinout and Pin Description

4.0.1 QFN64 Package

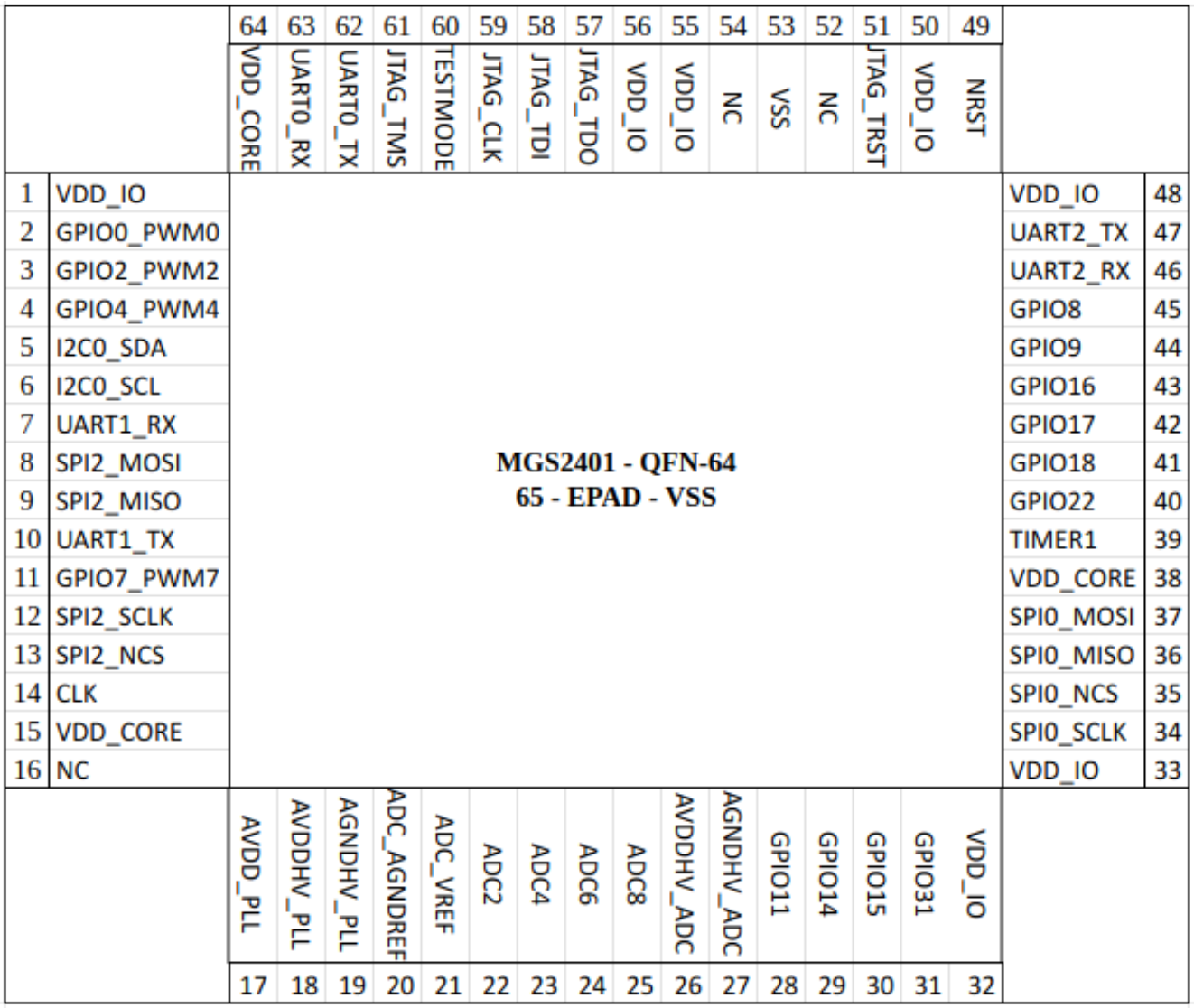

Figure 2: QFN64 Package

4.0.2 Pin and Ball Description

Pin Number (QFN)	Net Name
1	VDD_IO
2	GPIO0_PWM0
3	GPIO2_PWM2
4	GPIO4_PWM4
5	I2C0_SDA
6	I2C0_SCL
7	UART1_RX
8	SPI2_MOSI
9	SPI2_MISO
10	UART1_TX
11	GPIO7_PWM7
12	SPI2_SCLK
13	SPI2_NCS
14	CLK
15	VDD_CORE
16	NC
17	AVDD_PLL
18	AVDDHV_PLL
19	AGNDHV_PLL
20	ADC_AGNDREF
21	ADC_VREF
22	ADC2
23	ADC4
24	ADC6
25	ADC8
26	AVDDHV_ADC
27	AGNDHV_ADC
28	GPIO11
29	GPIO14
30	GPIO15
31	GPIO31
32	VDD_IO
33	VDD_IO

Pin Number (QFN)	Net Name
34	SPI0_SCLK
35	SPI0_NCS
36	SPI0_MISO
37	SPI0_MOSI
38	VDD_CORE
39	TIMER1
40	GPIO22
41	GPIO18
42	GPIO17
43	GPIO16
44	GPIO9
45	GPIO8
46	UART2_RX
47	UART2_TX
48	VDD_IO
49	NRST
50	VDD_IO
51	JTAG_TRST
52	NC
53	VSS
54	NC
55	VDD_IO_psram
56	VDD_IO
57	JTAG_TDO
58	JTAG_TDI
59	JTAG_CLK
60	TESTMODE
61	JTAG_TMS
62	UART0_TX
63	UART0_RX
64	VDD_CORE

Table 1: Pin and Ball Description

5 Module descriptions

5.1 Shakti C-Class Core

The C-class processor is a 64-bit controller designed for mid-range embedded applications. It supports the standard RV64GC instruction set architecture (ISA) extensions. It is a 6-stage In-Order pipeline core with Branch Prediction Unit (BPU), 16kB I-Cache, 16kB D-Cache. It also provides hardware performance monitoring counters for cache activity, pipeline stalls, branch behaviour, and arithmetic operations. For memory protection, the processor supports 8 entries of Physical Memory Protection (PMP) units , and includes a Translation Lookaside Buffer (TLB) with support for the SV39 Memory Management Unit (MMU). Additionally, the processor supports 4 RISC-V hardware triggers, selectable via the tselect register using indices 0–3. The core supports multiple privilege levels, including User Mode, Supervisor Mode, and Machine Mode. With MMU support, the processor can run operating systems such as Zephyr, FreeRTOS, and NuttX.

5.2 Peripherals

5.2.1 General-Purpose Input/Output (GPIO)

The device features 21 GPIO pins (`GPIO0`, `GPIO2`, `GPIO4`, `GPIO7`, `GPIO8`, `GPIO9`, `GPIO11`, `GPIO14`, `GPIO15`, `GPIO16 GPIO17`, `GPIO18`, `GPIO22`, `GPIO31 GPIO32`, `GPIO33`, `GPIO34`, `GPIO39`, `GPIO42`, `GPIO43`, and `GPIO44`). that can be individually configured as inputs or outputs, and designed to operate at 1MHz. Each pin also supports interrupt functionality.

Key Features

- **Individual Pin Control:**
  - **Set:** Sets the specified GPIO pin to HIGH logic level.
  - **Clear:** Sets the chosen GPIO pin to LOW logic level.
  - **Toggle:** Reverses the current logic level (HIGH to LOW or LOW to HIGH) on the designated GPIO pin.
- **Interrupt Handling:** GPIO pins can be configured to generate interrupts that are registered with the Peripheral Local Interrupt Controller (PLIC) for event-driven processing.

Pin Muxing with Pulse-Width Modulation (PWM)

- `GPIO0`, `GPIO2`, `GPIO4`, `GPIO7`, `GPIO17`, `GPIO18`, and `GPIO22` are pin-muxed with `PWM0`, `PWM2`, `PWM4`, `PWM7`, `PWM8`, `PWM9`, and `PWM13` respectively.
- This allows these pins to be configured for PWM generation, enabling precise control of parameters such as LED brightness or motor speed.

Note: Refer to the PWM chapter for detailed information on PWM configuration and usage.

Pin Muxing with Universal Asynchronous Receiver / Transmitter (UART)

- `GPIO8–GPIO9` are pin-muxed with `UART3 TX/RX`, and `GPIO11 and GPIO15` with `UART4 TX/RX` respectively.
- This enables serial communication with external devices.

Note: Refer to the UART chapter for detailed information on UART configuration and usage.

Pin Muxing with Serial Peripheral Interface (SPI)

- `GPIO32–GPIO34` are pin-muxed with `SPI2 (MOSI, MISO, NCS)` respectively.
- Enables high-speed serial communication with external peripherals such as sensors or memory devices.
- By default, these pins operate in SPI mode but can be reconfigured as GPIO if required.

Note: Refer to the SPI chapter for detailed information on SPI configuration and usage.

Pin Muxing with General-Purpose Timer (GPTimer)

- `GPIO39` is pin-muxed with `GPTIMER1` respectively.

- These pins can be used for event counting, pulse generation, or periodic signal timing.

Note: Refer to the GPTimer chapter for detailed information on GPTimer configuration and usage.

Pin Muxing with JTAG

- `GPIO42–GPIO44` are pin-muxed with `JTAG TDI, TMS, and TDO` respectively.
- Enables debugging and programming functionality.

Note: Refer to the JTAG chapter for detailed information.

5.2.2 ProIO

The **MGS2401 ProIO** feature of GPIO enables **high-speed parallel data transfers through GPIO pins**. Instead of toggling individual GPIOs in software, **ProIO** groups selected pins into fixed-width data buffers, allowing data to be captured or transmitted in parallel with minimal CPU involvement.

Each **ProIO** group operates with its own **FIFO and clocked data interface**, enabling efficient streaming of data between the MCU and external peripherals.

GPIO pins can be organized into the following ProIO groups:

- **Duo** – 2-bit data buffer
- **Tetra** – 4-bit data buffer

Key Features

- **High-Speed Data Transfer**
  - In **Input mode**, data is sampled from GPIO pins on each configured clock edge and stored in the buffer FIFO.
  - In **Output mode**, data is fetched from the FIFO and driven onto the GPIO pins in synchronization with the clock.
  - Enables **continuous, clock-synchronous data streaming** through GPIO.
  - Supports **DMA-based data transfers**, allowing the FIFO to be serviced automatically without CPU intervention.
- **Integrated FIFO**
  - Each ProIO group includes an internal FIFO to queue data.
  - Reduces software overhead by eliminating the need to service every GPIO transition.
- **Flexible Clocking**
  - Each group includes a **dedicated clock pin**.
  - Supports **internal clock generation with a configurable prescaler** or **external clock input**.
  - Allows easy interfacing with a wide range of peripheral data rates.
- **Configurable Data Groups**
  - Supports **2-bit (Duo) and 4-bit (Tetra)** configurations.
- **Selectable Data Access Width**
  - Data can be accessed using **8-bit, 16-bit, or 32-bit transfers**, enabling efficient CPU or DMA interaction.
- **Bidirectional Operation**
  - Groups can operate in:
    - **Input mode (Enqueue)** – capture data from GPIO pins into the FIFO.
    - **Output mode (Dequeue)** – transmit data from the FIFO to GPIO pins.
- **Configurable Clock Edge**
  - Data sampling or transmission can be triggered on either the **rising edge** or **falling edge** of the clock.

5.2.3 Pulse-Width Modulation (PWM)

This device provides 7 instances of PWM (`PWM0`, `PWM2`, `PWM4`, `PWM7`,`PWM8`,`PWM9` and `PWM13`). The following parameters can be configured for the PWM in Software.

- **Prescaler:** These bits select a division factor for the input clock to determine the PWM operating frequency.
- **Duty Cycle:** This register defines the on-time duration (duty cycle) of the PWM waveform as a percentage of the period.
- **Period:** This register sets the overall period of the PWM waveform, determining the frequency.
- **Complementary Output:** It is a functionality that generates an inverted version of the original Pulse Width Modulation (PWM) signal with a programmable dead time. This feature is commonly used for driving complementary MOSFETs in applications like:
  - **Gate Drive Circuits:** Driving the gates of high-side and low-side MOSFETs in a half-bridge configuration for motor control, DC-DC converters, and inverters.
  - **Synchronous Buck-Boost Converters:** Controlling the on/off states of synchronous rectifiers to achieve efficient power conversion.

5.2.4 Serial Peripheral Interface (SPI)

This device has 2 instances of SPI interfaces (`SPI0` and `SPI2`). Each SPI instance can support data transfers upto 35Mbps. The SPI is a synchronous serial I/O port that allows a serial bit stream of programmed length to be shifted into and out of the device at a programmable bit transfer rate. Each SPI module has four external pins - Master in/Slave out(MISO) pin, Master out/Slave in(MOSI) pin, Synchronous clock(SCLK) and Chip Select(CS) pin.

Key Features:

- The SPI peripheral can be configured as either Master or Slave.
- Each instance has interrupts registered with PLIC.

5.2.5 Quad Serial Peripheral Interface (QSPI)

The Quad-SPI (QSPI) module is a high-performance serial communication interface specifically designed for interfacing with external Quad-SPI flash memories. It offers significant advantages over traditional SPI for applications requiring high data throughput and large memory capacity. This device has 2 instances of QSPI interface.

Key Features:

- **Data Transfer:** QSPI utilizes four data lines (I0, I1, I2, I3) compared to the two data lines (MOSI and MISO) used in standard SPI. This quad-channel communication enables significantly faster data transfer rates upto 70Mbps in each data line.
- **Functional Modes:** The QSPI module offers two operational modes for flexible communication with external memory:
  - **Indirect Mode:** Provides complete control over data transfers using dedicated QSPI registers.
  - **Memory-Mapped Mode:** Maps the external memory to the microcontroller's address space, allowing direct access as if it were internal memory.
- **High-Speed Operation:** Supports Single Data Rate (SDR) mode for optimal data transfer speeds based on application requirements, with a maximum of 70MHz clock frequency, and does data-transfer upto 280Mbps.
- **Programmable Control:** Offers full programmability of opcodes and frame formats for both indirect and memory-mapped modes, ensuring adaptability to various flash memory protocols.
- **Efficient Data Handling:** Integrates FIFOs (First-In-First-Out) for both receive and transmit data paths, streamlining data flow and reducing CPU overhead.
- **Flexible Data Access:** Supports a wide range of data access sizes, including 8, 16, and 32 bits, for compatibility with diverse data types.
- **Comprehensive Interrupt Management:** Generates interrupts on various events, including FIFO threshold reached, timeout conditions, operation completion, and access errors, enabling efficient error handling and system monitoring.

- **Memory Mapped Region:** Supports upto 512 Megabytes storage in the memory-mapped mode for each instance of QSPI. The memory-mapped functional mode supports XIP mode, and RAM mode.
- **QSPI Interface Mapping:** In this part, QSPI0 and QSPI1 are internally mapped as follows:
  - QSPI0 → **8 Mbit Flash**
  - QSPI1 → **16 Mbit PSRAM**

5.2.6 Universal Asynchronous Receiver / Transmitter (UART)

This device has 5 UART interfaces (`UART0–UART4`). Each instance of the UART has interrupt lines that are connected to PLIC.

Key Features:

- The UART supports a wide range of communication speeds upto a baudrate of 1M.
- The UART0 is mapped as the serial console, while subsequent instances are exposed as IO pins.
- To provide more flexibility to the users, the following are software configurable:
  - Parity bit selection in both transmit and receive modes. The value of parity can be anything from 0-2.
  - Stop bits selection between 0-2 stop bits.
  - Character size configuration for character length transmission. It can support 5 to 8-bit characters.
- Has interrupts registered with PLIC for each instance of UART.

5.2.7 Inter-Integrated Circuit interface (I²C)

This device supports 1 I²C instance that operates at standard mode speed of upto 400 kHz and fast mode speed configurable upto 1MHz.

Key Features:

- The I²C instance supports only master mode operation, and does not work as a slave.
- The I²C instance supports multi-master mode.
- The I²C instance has an interrupt which is registered with PLIC.
- I²C instance supports 7-bit addressing mode, with maximum 128 slave devices.

5.2.8 Analog to Digital Converters (ADC)

The device has 1 instance of SAR ADC with 4 channels.

Key Features:

- The ADC has the resolution selectable between 12, 10, 8 and 6 bit.
- It has 5 MSPS Conversion Rate.
- The ADC supports 4 channels: `ADC2`, `ADC4`, `ADC6`, and `ADC8`.

5.2.9 JTAG

The device includes a single **JTAG DTM (Device Transport Module)** that enables JTAG communication with the chip. Through the JTAG interface, it is possible to connect to the processor's debugger, allowing enhanced debugging and development capabilities.

Key Features

- Supports JTAG communication speeds up to **10 MHz**.
- **TRST** (Test Reset) signal is supported.
- **Hardware breakpoints** are supported, enabling easier debugging through external debuggers.

5.2.10 Debugger

This module provides support to the user to check the system's state as required by the user, helping in debugging the system. This module can be accessed via the JTAG connection. This module is compliant with ratified RISC-V Debug Spec v0.13.

Key Features:

- Abstract command and system bus support.
- Can access the core registers, CSRs and memory mapped registers.
- Software breakpoints.

5.2.11 Processor Branch Trace

This module is used to get the program execution trace being a powerfull tool used for debugging user code. This module is compliant with RISC-V E-trace 2.0.0 spec. This module can be used when it is not possible to use a debugger to observe behaviour of a running system as this is intrusive. It is done by recording the discontinuties in the program execution address using the encoder and store the generated packets in a dedicated SRAM which afterwards is read by a host system and decoded to get the program execution trace.

Trace Encoder:

- The program execution trace is compressed into smaller packets/payloads using this module.

Key Features:

- The mandatory features mentioned in the RISC V E-trace spec are implemented.
- Additionally, filters are added. These filters can be used to record only necessary parts in a program execution trace. Has support of 3 filters.

Trace RAM sink:

- Once the encoder compresses the trace into smaller packets/payloads, they are written and stored in this RAM sink.
- The size of the RAM sink is 4kB. This trace RAM can then be read via the debugger via which we can extract the packets/payloads and get the trace after decoding.

Key Features:

- Has support for either wrap around or stop filling up the RAM once full.

5.2.12 General-Purpose Timer (GPTimer)

This device has 1 instance of GPTimer.

Key Features:

- Up, down, up-down counter.
- Simple PWM support.
- Timer capture support.

5.2.13 Watch-Dog Timer (WDTimer)

This device has 1 instance of WDTimer. This module can be used to come out of any system hang.

Key Features:

- Software controlled system reset
- Counter controlled system reset
- Interrupt mode

5.2.14 Platform Level Interrupt Controller (PLIC)

This device receives the interrupts from all the peripherals and notifies the system for an interrupt.

Key Features:

- Interrupt from 81 sources are connected.
- Interrupt priority value upto 7.
- A threshold register to service interrupts above a required priority value.

5.2.15 Direct Memory Access (DMA)

The Direct Memory Access (DMA) controller enables high-speed data transfers between memory and peripherals without continuous CPU intervention.

Key Features:

- Provides **8 independent channels**, which are serviced **sequentially** based on their assigned priority levels.
- Supports **memory-to-memory**, **peripheral-to-memory**, **peripheral-to-peripheral** and **memory-to-peripheral** transfer modes.
- Each channel supports data widths of **8-bit**, **16-bit**, **32-bit**, or **64-bit**.
- Each channel supports **four priority levels (0–3)** .

5.2.16 Pin Multiplexing (PINMUX)

Pinmux (Pin Multiplexing) is a mechanism that allows a single physical pin to support multiple alternate functions.

Key Features

- Allows a **single pin to support multiple alternate peripheral functions**.
- Enables configuration of pins for interfaces such as **GPIO, UART, GPTimer, JTAG, SPI and PWM**.
- Only **one function can be active on a pin at a time** to avoid peripheral conflicts.

Pinmux Register Map

Register Name	Offset (Hex)	Function when clear	Function when set
MUX0	0x0000	GPIO0	PWM0
MUX2	0x0008	GPIO2	PWM2
MUX4	0x0010	GPIO4	PWM4
MUX7	0x001C	GPIO7	PWM7
MUX8	0x0020	GPIO17	PWM8
MUX9	0x0024	GPIO18	PWM9
MUX13	0x0034	GPIO22	PWM13
MUX14	0x0038	SPI2_MOSI	GPIO32
MUX15	0x003C	SPI2_MISO	GPIO33
MUX16	0x0040	SPI2_NCS	GPIO34
MUX20	0x0050	GPIO8	UART3_TX
MUX21	0x0054	GPIO9	UART3_RX
MUX22	0x0058	GPIO11	UART4_TX
MUX23	0x005C	GPIO15	UART4_RX
MUX25	0x0064	GPTIMER1	GPIO39
MUX28	0x0070	JTAG_TDI	GPIO42
MUX29	0x0074	JTAG_TMS	GPIO43
MUX30	0x0078	JTAG_TDO	GPIO44

Table 2: Pin Functions

5.3 Security accelerators

This microcontroller integrates a powerful suite of security accelerators designed to safeguard your applications and data. These accelerators offload computationally intensive cryptographic operations from the main CPU, enabling:

- **Reduced Power Consumption:** By offloading encryption and decryption tasks to dedicated hardware, power usage associated with these security operations can be minimized, extending battery life in portable devices.
- **Enhanced Security:** The dedicated security accelerators free up valuable CPU resources, allowing the main processor to concentrate on core application functionalities while ensuring robust cryptographic operations in the background.

The following industry-standard algorithms are supported in hardware.

5.3.1 RSA

This versatile public-key cryptography algorithm is widely used for digital signatures and secure key exchange. Hardware acceleration significantly improves the performance of RSA encryption and decryption operations, especially for larger key sizes like 2048 bits, which offer a high level of security.

The on-board RSA accelerator supports 2048 bit keys.

5.3.2 AES

This widely adopted symmetric key algorithm is a cornerstone of modern cryptography. AES hardware acceleration empowers you to encrypt and decrypt data efficiently, protecting sensitive information at rest and in transit. This device has support for AES 128,192,256 with Cipher Block Chaining mode, Cipher FeedBack mode, Output FeedBack mode and Counter mode.

5.3.3 SHA-2

This cryptographic hash function generates a unique and fixed-size fingerprint from a data stream. Hardware acceleration for SHA256 enables efficient message integrity verification and digital signature validation, ensuring data authenticity and tamper detection.

5.3.4 One-Time Programmable Memory (OTP Memory)

The device has 32 Kbit of OTP that provides secure storage for sensitive data like cryptographic keys. It is also used for Secure-Boot of MGS2401. This tamper-resistant memory ensures the confidentiality and integrity of your sensitive information.

5.3.5 True Random Number Generator (TRNG)

The device has a single instance of NIST SP800-90C compliant True Random Number Generator. This hardware module generates unpredictable numbers essential for cryptographic operations, strengthening the overall security posture of your system.

Key Features:

- Background noise collection to speed reseeding operations.
- Entropy Dispatch Unit (EDU) to provide multi-master support, serial entropy streams, and ESM nonce port.
- Internal random seeding operation.
- 128-bit random number generation.
- Start-up, continuous and on-demand health tests.
- Compliant with NIST SP800-90A/B/C and BSI AIS 20/31.
- 128-bit or 256-bit of security strength.
- Ring oscillator-based Bit Generator blocks with wide system clock rate dynamic range.

5.4 Pin Functions

Signal	Function	I/O	Description
PLL_VREF	Analog Signal	Input	External voltage reference for PLL. Connect it to VDD_IO.
ADC_DISLVL	Analog Signal	Input	Analog input output.
CLK	Clock	Input	External reference clock (20MHz).
SPIx_SCLK	SPI	Output	Provides the clock signal that synchronizes data transfer between the master and slave devices.
SPIx_NCS	SPI	Output	Used by the master to select a specific slave device. A low signal on this pin selects the slave.
SPIx_MISO	SPI	Input	Carries data from the slave device to the SPI master.
SPIx_MOSI	SPI	Output	Carries data from the SPI master to the slave device.
I2C_SDA	I2C	Open-Drain	This pin acts as the input and output during data transfer w.r.t I2C_SCL.
I2C_SCL	I2C	Open-Drain	Provides I2C clock signal that synchronizes data transfer between the slave device.
ADCx	ADC	Input	Single ended input with 8/10/12 bit resolution.
GPIOx/PWMx	GPIO/PWM	Inout	General purpose Input and output pinmuxed with PWM.
GPIOx	GPIO	Inout	General purpose Input and output.
TIMER	GPTIMER	Inout	Timer Interrupt.
TDI	JTAG	Input	Test Data Input.
TDO	JTAG	Output	Test Data Output pin that carries data out from the JTAG interface of the device being tested.
TMS	JTAG	Input	Controls the operational state of the JTAG interface by applying a specific sequence of logic levels.
TCK	JTAG	Input	Provides the clock signal that synchronizes data transfer on the TDI and TDO lines.
TRST	JTAG	Input	Pin can be tied to high with Vref.
UARTx_TX	UART	Output	Transmit data.
UARTx_RX	UART	Input	Receive data.

Note: The ‘x’ present in SPIx, GPIOx, PWMx, UARTx and ADCx specifies the instance number for each peripheral. Can be used as , SPI1, UART2 etc. I2C works based on open drain/emulator configuration.

6 Boot Configuration

Mindgrove Silicon's MGS2401Q64CF8R16 provides Secure-Boot capability. The boot configuration is stored in the on-chip Boot-ROM.

6.1 Boot Modes Supported

1. Secure-Boot with QSPI0.
2. Normal-Boot with QSPI0.
3. Parking Loop if QSPI0 is not available.

6.2 Prerequisites for Boot

For successful booting of the software application, in modes 1 and 2, the following are expected to be present.

1. QSPI Flash connected to QSPI0 interface, programmed with valid software application. The flash must be capable of supporting XIP (eXecute In Place) mode. It is requested because, QSPI0 will change its mode to XIP, in which the programs starts executing from the flash memory, rather than copying it into the RAM and running.
2. UART0 is set as the Serial Output by default, and cannot be changed by the user. The baudrate to be set in the Serial-Terminal to view the output should be 115200.

6.3 Boot Process

Upon powering on or resetting, the MGS2401Q64CF8R16 begins by reading OTP memory to check the `JTAG_LOCK` bit, locking the JTAG interface if set, or leaving it open for development if not.

The system then probes QSPI0 for a valid SFDP response, falling back to QSPI1 if needed. If neither interface yields a valid flash device, the system sets `BOOT_STATUS: NO_FLASH` and halts.

Once a flash source is confirmed, the bootloader checks for a custom QSPI configuration header. It applies custom XIP settings to flash if custom QSPI configuration header is found, or falls back to default XIP settings otherwise.

It then reads the application image size. If the size exceeds 16 MB, the system halts with `BOOT_STATUS: INVALID APP LEN`.

A validity check on the application entry point is then performed, which triggers `BOOT_STATUS: NO_APPLN` and a halt if an invalid pattern is detected.

If the application headers are valid, the bootloader consults OTP to determine whether secure boot is enabled. If not, the application executes directly.

If secure boot is enabled, the bootloader reads public key data from OTP, blocking debug access. If no key or an invalid key is found in OTP, the core stalls with `ERR_CODE: NO PUB KEY` or `ERR_CODE: INVALID PUB KEY`.

It then verifies PKCS #1 v1.5 padding in the decrypted signature and compares the runtime SHA hash against the signed hash. On failure, the system halts with `ERR_CODE: RSA_PKCS_DECRYPT` or `ERR_CODE: SHA_MISMATCH`, respectively.

A fully successful secure boot proceeds to application execution.

Should an exception occur at any point during execution, the trap handler logs the `mcause` and `mepc` registers and halts in a while loop.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Paramter	Symbol	Description	Min	Typ	Max
Supply Voltage	VDD_CORE	Maximum voltage that can be applied to the power supply pins.	0.81V	0.9V	0.99V
Input/Output Voltage	VDD_IO	Maximum voltage that can be applied to input/output pins.	1.62V	1.8V	1.98V
Reference power supply voltage	PLL_VREF	External voltage reference for PLL.	0.81V	0.9V	0.99V
Analog power supply voltage	AVDD_PLL	Analog 0.9V power supply for PLL.	0.81V	0.9V	0.99V
Analog power supply voltage	AGND_PLL	Dedicated Analog ground for PLL 0.9V supply.	0.81V	0.9V	0.99V
Analog power supply voltage	AVDDHV_PLL	Dedicated Analog 1.8V power supply for PLL.	1.62V	1.8V	1.98V
Analog power supply voltage	AGNDHV_PLL	Dedicated Analog ground for PLL 1.8V supply.	1.62V	1.8V	1.98V
Load capacitance	(C)	Capacitance.	5pF	-	25pF

Table 4: Absolute Maximum Ratings

7.2 Operating Conditions

TBD

7.3 Power Consumption

TBD

7.4 Thermal Characteristics

Paramater	Symbol	Description	Min	Typ	Max
Operating Temperature	(Tj)	Temperature range for safe device operation.	-40°C	25°C	+85°C

Table 5: Thermal Characteristics

7.5 Timing

TBD

8 PCB Guidelines

- All capacitors for the supply VDD_CORE, VDD_IO, AVDDHV_ADC, AVDD_PLL, AVDDHV_PLL must be as close as possible to the respective pins. The smallest capacitors must be the closest to the package pins.

8.1 PLL

- Place capacitors between (typically 0.1uF ceramic) AVDD_PLL to gnd. Power pins should be close to capacitors.
- External supply noise should be kept to a minimum, and special care should be taken to avoid low frequency (<1MHz) ripple noise content, for example originated from low frequency power management events or DC-DC conversion.
- The clock trace should be well isolated from other noisy PCB traces.
- Prioritize placing the crystal oscillator in close proximity to the relevant input and output pins.
- Avoid placing clock lines and switching signal lines near crystals and their connections.

8.2 ADC

- Place 0.01- F bypass capacitor between AVDDHV_ADC to gnd.
- All capacitors for ADC1-8, ADC_VREF must be as close as possible to the respective package pins.
- ADC1-8 lines must be shielded.
- To enable/diable ADC, it can be tied to low/high in the PCB respectively.

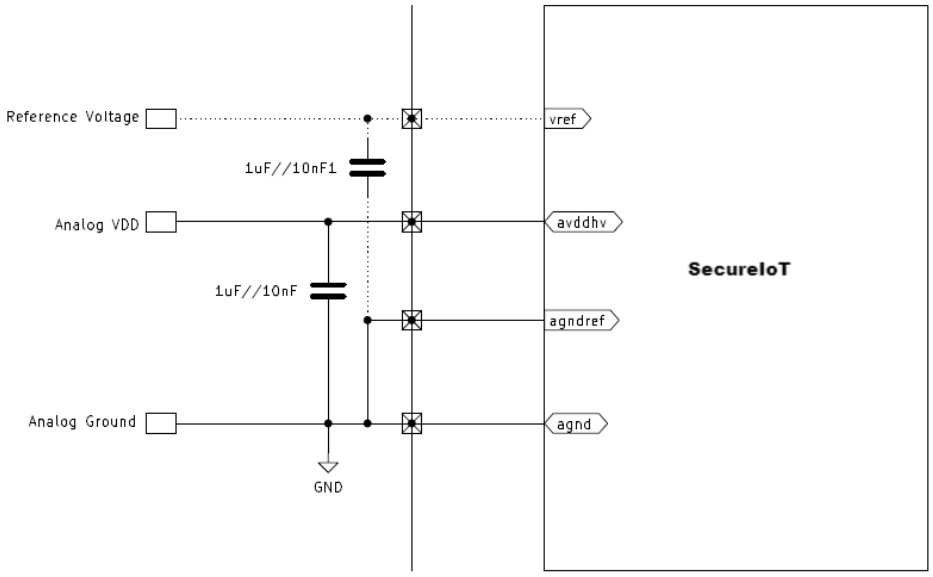

Figure 3: ADC Decoupling Schematic

8.3 I2C

- Pull-up resistors are used to keep the SDA and SCL lines at a high voltage level when they are not being driven by the devices.

- I2C bus loads should be kept to a minimum to reduce the number of devices. Signal degradation and communication problems may occur if too many devices are connected to the bus.
- Avoid routing high speed signals near the SDA and SCL traces.

8.4 JTAG

- Keep JTAG traces (TCK, TMS, TDI, TDO, TRST*) as short as possible, especially between the JTAG connector and the first JTAG-enabled device. This reduces signal delay and minimizes noise pickup.
- Matched lengths between the JTAG header and each device's JTAG pins. This ensures signals arrive simultaneously for proper operation.
- Provide a dedicated ground plane for JTAG signals to minimize noise. Connect this plane to the system ground at a single point to avoid ground loops.

9 Software and Tools

9.1 SDK

The software development kit (SDK) provides the tools required for baremetal software development. The SDK includes the baremetal library which contains the peripheral drivers, and example programs for peripherals like UART, GPIO, ProIO, I2C, SPI, QSPI, PWM etc., along with some application drivers such as LCD, RTC etc. The SDK also includes the drivers and example programs for hardware based crypto-accelerators like AES, SHA, RSA etc.

9.1.1 Tools Required

1. RISC-V GNU Toolchain - for compiling and debugging.
2. Open On Chip Debugger - for JTAG based debugging.
3. Serial Terminal (e.g., GTKTerm, puTTY) - for viewing outputs.

Note: The SDK can be accessed upon request.

9.2 IDEs

The supported IDEs for software development include the following:

- Microsoft Visual Studio Code,
- Eclipse

The provided code examples can be run using these IDEs.

9.3 RTOSs

Currently, the following RTOSs have been tested with MGS2401:

- FreeRTOS
- Zephyr OS
- NuttX

For the above mentioned Real-Time Operating Systems, all the peripheral drivers are included.

10 Package Information

10.1 QFN64

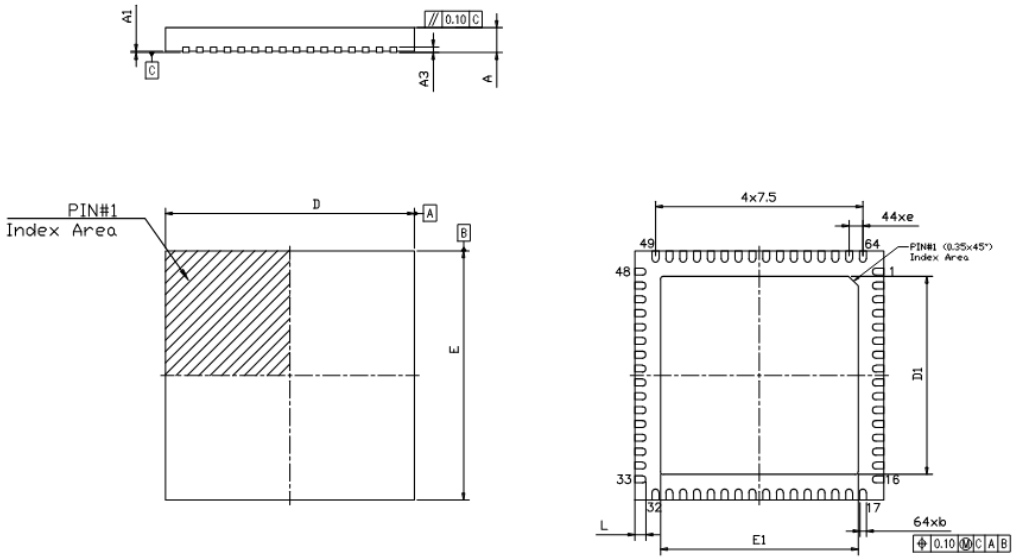

Figure 4: QFN64 Package

COMMON DIMENSION (mm)

Symbol	MIN	NOM	MAX
b	0.20	0.25	0.30
D	8.90	9.00	9.10
E	8.90	9.00	9.10
L	0.30	0.40	0.50
e		0.50 BSC	
A1	0.00	0.02	0.05
A	0.85	0.90	0.90
A3		0.203 REF	

Table 6: QFN64 COMMON DIMENSION

EPAD OPTION

Symbol	MIN	NOM	MAX
D1	7.05	7.15	7.25
E1	7.05	7.15	7.25

Table 7: QFN64 EPAD OPTION

Note:
1. All dimensions are in mm, angles in Degrees.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Coplanarity applied to the exposed pad as well as the terminals.
4. Coplanarity 0.1mm.
5. Warpage shall not exceed 0.1mm.
6. Pin location is identified by chamfer.
7. Lead width, lead thickness exclusive of solder plate.
8. Package outline exclusive of mold flashes and burr dimensions.

11 Glossary and references

- RISC-V International: https://riscv.org/
- SHAKTI Processor: https://shakti.org.in
- RISC-V ISA Specifications:
  - Unprivileged Specification
  - Privileged Specification
- RISC-V Non-ISA Specifications:
  - Efficient Trace
  - RISC-V ABIs
  - RISC-V Debug
  - RISC-V Platform Level Interrupt Controller
  - RISC-V Supervisor Binary Interface
- OCSRAM: On-chip SRAM
- OTP Memory: One-Time Programmable Memory

12 Revision History

Rev. No	Date	Description	Modified by	Approved by
1.0	03-06-2024	Initial revision for Secure IoT MPW	M. Kapil Shyam	Shashwath T.R.
1.1	09-09-2024	Updated PCB Layout Guidelines	Swaathi S	Shashwath T.R.
1.2	27-12-2024	Updated Part code ordering info	Mouna Krishna	Shashwath T.R.
2.0	27-03-2026	Updated Boot Sequence, ProIO details, Package details	Deeptha G	M. Kapil Shyam

Table 8: Revision history

