MGS2401B144C

Technical Datasheet

MINDGROVE

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Contents

1 Product overview

Mindgrove Silicon's MGS2401 is a high performance microcontroller targeting the IoT and embedded domains. It offers optimized power consumption at a high clock frequency with a large number of I/Os and peripherals. Also included is a security complex that accelerates cryptographic algorithms and stores secure information such as cryptographic keys.

1.1 Features

- Compute core:
  - 1x Shakti C-Class 64 bit RISC-V core
  - 6-stage In-Order operation
  - RV64GC (RV64IMAFDC)
  - 16kB I-Cache
  - 16kB D-cache
  - 4 PMP entries
  - 700 MHz clock frequency
- 128 kB on-chip SRAM (OCSRAM)
- Peripherals
  - 2xQSPI
    - Supports SDR Mode
    - XIP Mode
    - RAM Mode
    - Has Interrupt functionality
  - 4xSPI
    - Can be configured as Master/Slave
    - Data transfers upto 35Mbps
    - Compliant with JESD251C
    - Has Interrupt functionality
  - 2xI2C
    - Supports only Master mode
    - Standard Mode (upto 100 kHz)
    - Fast Mode (upto 400 kHz)
    - High Speed Mode (upto 1MHz)
    - Has Interrupt functionality
  - 5xUART
    - Supports 5 to 8-bit character transfer/receive
    - TX/RX buffer interrupts
    - Supports 1-bit even/odd parity
    - Supports 1/1.5/2 stop bits
  - 45xGPIO
    - Rated to work at 1MHz.
    - 14-GPIOs Multiplexed with PWMs
    - 4-GPIOs Multiplexed with UARTs.
    - 6-GPIOs Multiplexed with SPIs.
    - 4-GPIOs Multiplexed with GPTimers.
    - 3-GPIOs Multiplexed with JTAG.
  - 14xPWM
    - Counter Reset
    - Complementary Output
    - Rise/Fall Interrupt
    - Half Period Interrupt
  - 1xADC
    - 12-Bit Successive Approximation Register (SAR) ADC
    - 8 Channels
    - 5MSPS Conversion Rate
    - 8:1 Multiplexed Inputs
  - 4xGPTimer
  - 1xWatchdog Timer
  - 1xPLIC
  - 1xCLINT
  - 1xDMA
    - 8 independent channels.
- Security
  - Hardware Crypto Accelerators
    - AES
      - Supports 128, 192, 256 Bits
      - Supports CBC, CFB, OFB, CTR modes
    - RSA 2048
    - SHA 2 - 256
    - True Random Number Generator
  - On-chip secure memory
    - 4kB on-chip OTP memory
  - Secure Boot
- Operating voltage
  - Core: 0.9V
  - I/O: 1.8V
- Packages:
  - 144-Pin WBGA Package, 0.5-mm Ball Pitch

2 Ordering Information

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact MG sales office.

2.1 Ordering Code Format

```
MG{SocName}-{PackageDetails}{TemperatureGrade}{CoPackageDetails}-{PackageType}
      |         |                |                 |              |
      |         |                |                 |              └─> [Package Type]
      |         |                |                 └────────────────> [Co-Package Details]
      |         |                └──────────────────────────────────> [Temperature Grade]
      |         └───────────────────────────────────────────────────> [Package Details]
      └─────────────────────────────────────────────────────────────> [SoC Name]
```

2.1.1 Code Breakdown

- **Device Family:** MGS = MindGrove silicon SecureIoT
- **Package Details:**
  - **B144** – BGA 144 pins
  - **Q64** – QFN 64 pins
- **Co-Package Details:**
  - **F8R8** – Flash: 8 Mbit, PSRAM: 8 Mbit
  - **F8R16** – Flash: 8 Mbit, PSRAM: 16 Mbit
  - **F16** – Flash: 16 Mbit
  - **F02** – Flash: 256 Kbit
- **Temperature Grade:**
  - **C** – Consumer (0 °C to +85 °C)
- **Package Type:**
  - **T** – Tape
  - **R** – Reel
  - **B** – Tray

2.2 Example Ordering Code

`MGS2401-B144C-B`

`MGS2401-Q64C-F8R16-B`

3 Block diagram

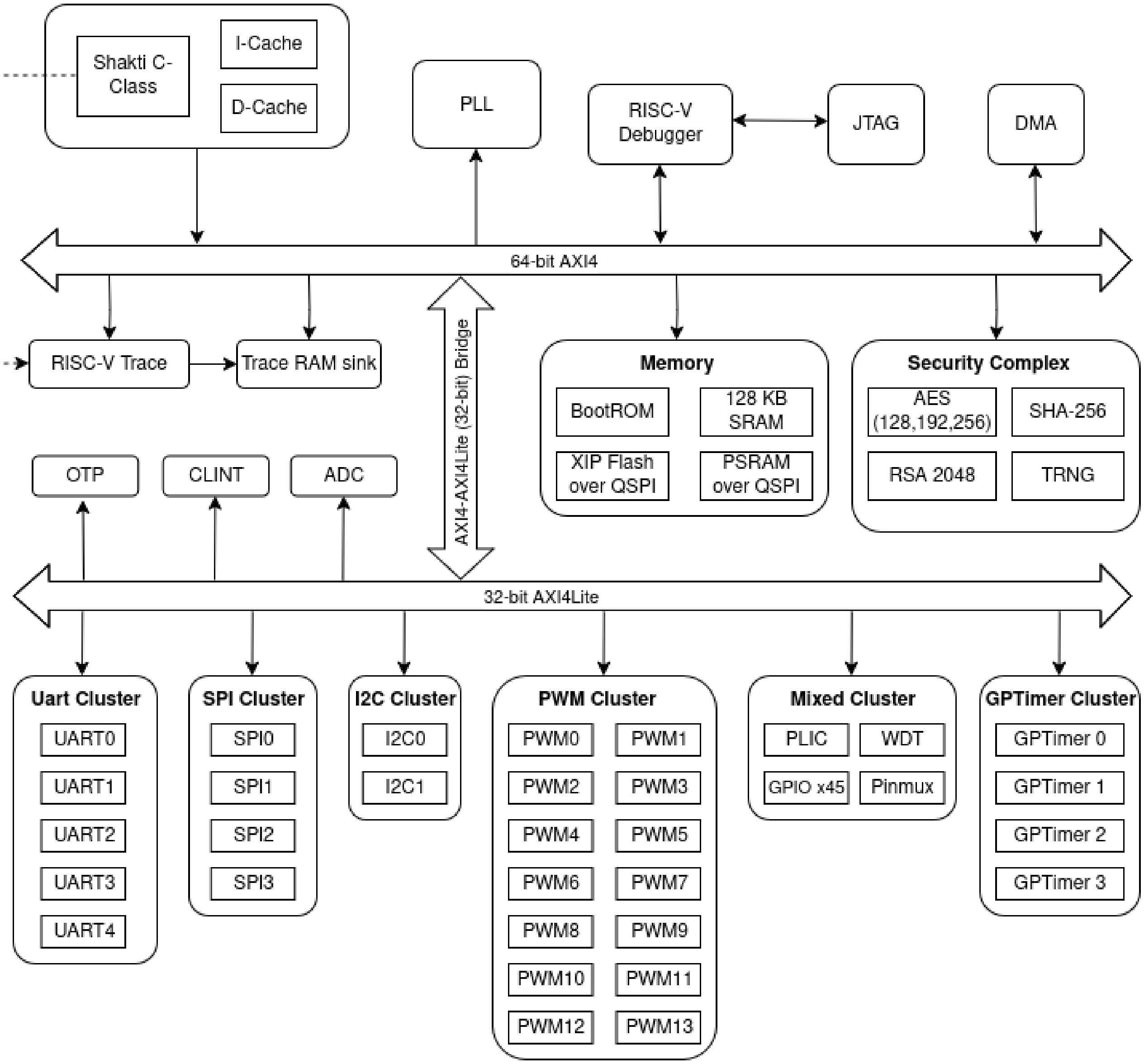

Figure 1: MGS2401 Block Diagram

4 Pinout and Pin Description

4.0.1 WBGA144 Package

Ball#	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	UART0_Tx	UART0_Rx	JTAG_TMS	VSS	SPI3_SCLK	SPI3_MOSI	SPI3_MISO	VSS	I2C1_SCL	I2C1_SDA	VSS
B	SPI1_MOSI	SPI1_SCLK	SPI1_MISO	TESTMODE	JTAG_TDI	SPI3_nCS	QSPI1_IO3	QSPI1_nCS	TIMER3	JTAG_TRST	GPIO8	GPIO20
C	GPIO0	VSS	SPI1_nCS	VSS	TIMER2	JTAG_TDO	QSPI1_CLK	QSPI1_IO2	QSPI1_IO0	VSS	UART2_Rx	UART2_Tx
D	QSPI0_IO2	GPIO3	GPIO1	VSS	VDDIO	JTAG_TCK	VSS	QSPI1_IO1	GPIO10	nRST	GPIO9	GPIO17
E	QSPI0_IO1	GPIO2	GPIO4	VDDIO	VSS	VDDIO	VSS	VDDIO	GPIO23	GPIO21	GPIO16	GPIO18
F	I2C0_SDA	VSS	I2C0_SCL	GPIO5	VDDCORE	VSS	VDDCORE	VSS	VDDIO	VSS	TIMER1	GPIO19
G	QSPI0_nCS	QSPI0_IO3	UART1_Rx	VDDIO	VSS	VDDCORE	VSS	VDDIO	GPIO25	GPIO24	TIMER0	GPIO22
H	GPIO6	SPI2_MOSI	QSPI0_IO0	UART1_Tx	VDDCORE	VSS	VDDCORE	VSS	GPIO27	GPIO29	GPIO26	GPIO28
J	SPI2_MISO	VSS	QSPI0_CLK	VDDIO	VSS	VDDIO	VSS	VDDIO	GPIO11	GPIO12	SPI0_nCS	SPI0_MOSI
K	SPI2_nCS	GPIO7	SPI2_SCLK	CLK	ADC_Vref	ADC_DISLVL	ADC0	ADC4	AVDDHV_ADC	GPIO13	SPI0_SCLK	SPI0_MISO
L	AVDD_PLL	AGND_PLL	AGNDHV_ADC	AVDDHV_ADC	AGNDHV_ADC	ADC_VBG	ADC6	ADC2	AGNDHV_ADC	VSS	GPIO31	GPIO30
M	AGND_PLL	AVDD_PLL	PLL_Vref	AVDDHV_PLL	ADC_AGNDref	ADC1	ADC3	ADC5	ADC7	GPIO15	GPIO14	VSS

Figure 2: WBGA144 Pin Diagram

4.0.2 Pin and Ball Description

Pin Number (BGA)	Net Name
A1	VSS
A2	UART0_TX
A3	UART0_RX
A4	JTAG_TMS
A5	VSS
A6	SPI3_SCLK
A7	SPI3_MISO
A8	SPI3_MOSI
A9	VSS
A10	I2C1_SCL
A11	I2C1_SDA
A12	VSS
B1	SPI1_MOSI
B2	SPI1_SCLK
B3	SPI1_MISO
B4	TESTMODE
B5	JTAG_TDI
B6	SPI3_NCS
B7	QSPI1_IO[3]
B8	QSPI1_IO[1]
B9	TIMER3
B10	JTAG_TRST
B11	GPIO8
B12	GPIO20
C1	GPIO0
C2	VSS
C3	SPI1_NCS
C4	VSS
C5	TIMER2
C6	JTAG_TDO
C7	QSPI1_CLK
C8	QSPI1_IO[2]
C9	QSPI1_IO[0]

Pin Number (BGA)	Net Name
C10	VSS
C11	UART2_RX
C12	UART2_TX
D1	QSPI0_IO[2]
D2	GPIO3
D3	GPIO1
D4	VSS
D5	VDD_IO
D6	JTAG_CLK
D7	VSS
D8	QSPI1_IO[1]
D9	GPIO10
D10	NRST
D11	GPIO9
D12	GPIO17
E1	QSPI0_IO[1]
E2	GPIO2
E3	GPIO4
E4	VDD_IO
E5	VSS
E6	VDD_IO
E7	VSS
E8	VDD_IO
E9	GPIO23
E10	GPIO21
E11	GPIO16
E12	GPIO18
F1	I2C0_SDA
F2	VSS
F3	I2C0_SCL
F4	GPIO5
F5	VDD_CORE
F6	VSS
F7	VDD_CORE
F8	VSS

Pin Number (BGA)	Net Name
F9	VDD_IO
F10	VSS
F11	TIMER1
F12	GPIO19
G1	QSPI0_NCS
G2	QSPI0_IO[3]
G3	UART1_RX
G4	VDD_IO
G5	VSS
G6	VDD_CORE
G7	VSS
G8	VDD_IO
G9	GPIO25
G10	GPIO24
G11	TIMER0
G12	GPIO22
H1	GPIO6
H2	SPI2_MOSI
H3	QSPI0_IO[0]
H4	UART1_TX
H5	VDD_CORE
H6	VSS
H7	VDD_CORE
H8	VSS
H9	GPIO27
H10	GPIO29
H11	GPIO26
H12	GPIO28
J1	SPI2_MISO
J2	VSS
J3	QSPI0_CLK
J4	VDD_IO
J5	VSS
J6	VDD_IO
J7	VSS

Pin Number (BGA)	Net Name
J8	VDD_IO
J9	GPIO11
J10	GPIO12
J11	SPI0_NCS
J12	SPI0_MOSI
K1	SPI2_NCS
K2	GPIO7
K3	SPI2_SCLK
K4	CLK
K5	ADC_VREF
K6	ADC_DISLVL
K7	ADC1
K8	ADC5
K9	AVDDHV_ADC
K10	GPIO13
K11	SPI0_SCLK
K12	SPI0_MISO
L1	AVDD_PLL
L2	AGND_PLL
L3	AGNDHV_PLL
L4	AVDDHV_ADC
L5	AGNDHV_ADC
L6	ADC_VBG
L7	ADC7
L8	ADC3
L9	AGNDHV_ADC
L10	VSS
L11	GPIO31
L12	GPIO30
M1	AGND_PLL
M2	AVDD_PLL
M3	PLL_VREF
M4	AVDDHV_PLL
M5	ADC_AGNDREF
M6	ADC2

Pin Number (BGA)	Net Name
M7	ADC4
M8	ADC6
M9	ADC8
M10	GPIO15
M11	GPIO14
M12	VSS

Table 1: Pin and Ball Description

5 Memory Map

The following table describes the memory map of the Mindgrove Silicon's MGS2401. The addresses are given in hexadecimal format.

Note: The internal fields inside each block/peripheral may be Read-Only or Write-Only. Refer to each Block's/Peripheral's Description in the user manual for more details.

Start Address	End Address	Peripherals	Size (Bytes)
0x00000010	0x0000001F	Debugger	16
0x00001000	0x00002FFF	Boot Space	8K
0x00009000	0x0000FFFF	TRNG	28K
0x00011300	0x00011340	UART0	64
0x00011400	0x00011440	UART1	64
0x00011500	0x00011540	UART2	64
0x00011600	0x00011640	UART3	64
0x00011700	0x00011740	UART4	64
0x00020000	0x000200FF	SPI0	256
0x00020100	0x000201FF	SPI1	256
0x00020200	0x000202FF	SPI2	256
0x00020300	0x000203FF	SPI3	256
0x00030000	0x000300FF	PWM0	256
0x00030100	0x000301FF	PWM1	256
0x00030200	0x000302FF	PWM2	256
0x00030300	0x000303FF	PWM3	256
0x00030400	0x000304FF	PWM4	256
0x00030500	0x000305FF	PWM5	256
0x00030600	0x000306FF	PWM6	256
0x00030700	0x000307FF	PWM7	256
0x00030800	0x000308FF	PWM8	256
0x00030900	0x000309FF	PWM9	256
0x00030A00	0x00030AFF	PWM10	256
0x00030B00	0x00030BFF	PWM11	256
0x00030C00	0x00030CFF	PWM12	256
0x00030D00	0x00030DFF	PWM13	256
0x00032000	0x000320FF	ADC	256
0x00033000	0x000330FF	OTP Memory	256
0x00040000	0x000400FF	QSPI0	256

Start Address	End Address	Peripherals	Size (Bytes)
0x00040100	0x000401FF	QSPI1	256
0x00040200	0x000403FF	GPIO 0..44	256
0x00040400	0x000403FF	Pinmux Registers	256
0x00040500	0x00040420	WDTimer	32
0x00044000	0x000440FF	I2C0	256
0x00044100	0x000441FF	I2C1	256
0x00044200	0x0004421F	GPTimer0	32
0x00044220	0x0004423F	GPTimer1	32
0x00044240	0x0004425F	GPTimer2	32
0x00044260	0x0004427F	GPTimer3	32
0x00060000	0x000600FF	I-Trace	256
0x00060100	0x000601FF	I-Trace RAM	256
0x00100000	0x0010FFFF	PLL	32K
0x02000000	0x020BFFFF	CLINT	786K
0x03000000	0x030000FF	SHA256	256
0x04000000	0x040000FF	AES	256
0x05000000	0x050000FF	RSA2048	256
0x07000000	0x070001FF	DMA	4K
0x0C000000	0x0FFFFFFF	PLIC	67M
0x80000000	0x8001FFFF	Memory Space	128K
0x90000000	0xAFFFFFFF	XIP0	512M
0xB0000000	0xCFFFFFFF	XIP1	512M

Table 2: Memory Map

6 Module descriptions

6.1 Shakti C-Class Core

The C-class processor is a 64-bit controller designed for mid-range embedded applications. It supports the standard RV64GC instruction set architecture (ISA) extensions. It is a 6-stage In-Order pipeline core with Branch Prediction Unit (BPU), 16kB I-Cache, 16kB D-Cache. It also provides hardware performance monitoring counters for cache activity, pipeline stalls, branch behaviour, and arithmetic operations. For memory protection, the processor supports 4 entries of Physical Memory Protection (PMP) units , and includes a Translation Lookaside Buffer (TLB) with support for the SV39 Memory Management Unit (MMU). Additionally, the processor supports 4 RISC-V hardware triggers, selectable via the tselect register using indices 0–3. The core supports multiple privilege levels, including User Mode, Supervisor Mode, and Machine Mode. With MMU support, the processor can run operating systems such as Zephyr, FreeRTOS, and NuttX.

6.1.1 Physical Memory Protection (PMP)

Physical Memory Protection (PMP) provides a hardware mechanism to control access to physical memory by software executing on a hart. PMP allows privileged software to define memory regions with configurable read, write, and execute permissions. These permissions are selectively enforced by hardware based on the configured PMP entries and privilege mode. The S2401 supports a minimum PMP granularity of 8 bytes and provides 4 configurable PMP entries.

Key Features

- **Configuration:** S2401 provides **4 configurable PMP entries** with a minimum PMP granularity of **8 bytes**. The PMP address is right-shifted by 3 bits (LSB 3 bits must be zero).
- **Matching Modes:** The PMP module supports two address matching modes for flexible memory region protection:
  - **TOR (Top Of Range):** Protects the address range between consecutive PMP addresses. `pmpaddr0` protects from `0x00000000` to `pmpaddr0`; `pmpaddr1` protects from `pmpaddr0` to `pmpaddr1`, and so on.
  - **NAPOT (Naturally Aligned Power Of Two):** Protects naturally aligned regions of power-of-two size (minimum 8 bytes). Region size expands by appending 1's from bit 4 of the address upward, terminated by a 0.

6.2 Peripherals

6.2.1 General-Purpose Input/Output (GPIO)

The device features 32 GPIO pins that can be individually configured as inputs or outputs, and designed to operate at 1MHz. Each pin also supports interrupt functionality.

Key Features

- **Individual Pin Control:**
  - **Set:** Sets the specified GPIO pin to HIGH logic level.
  - **Clear:** Sets the chosen GPIO pin to LOW logic level.
  - **Toggle:** Reverses the current logic level (HIGH to LOW or LOW to HIGH) on the designated GPIO pin.
- **Interrupt Handling:** GPIO pins can be configured to generate interrupts that are registered with the Peripheral Local Interrupt Controller (PLIC) for event-driven processing.

Pin Muxing with Pulse-Width Modulation (PWM)

- The first eight GPIO pins (`GPIO0–GPIO7`) are pin-muxed with their corresponding PWM channels (`PWM0–PWM7`), while GPIO pins (`GPIO17–GPIO22`) are pin-muxed with PWM channels (`PWM8–PWM13`) respectively.
- This allows these pins to be configured for PWM generation, enabling precise control of parameters such as LED brightness or motor speed.

Note: Refer to the PWM chapter for detailed information on PWM configuration and usage.

Pin Muxing with Universal Asynchronous Receiver / Transmitter (UART)

- `GPIO8–GPIO9` are pin-muxed with `UART3 TX/RX`, and `GPIO11 and GPIO15` with `UART4 TX/RX` respectively.
- This enables serial communication with external devices.

Note: Refer to the UART chapter for detailed information on UART configuration and usage.

Pin Muxing with Serial Peripheral Interface (SPI)

- `GPIO32–GPIO34` are pin-muxed with `SPI2 (MOSI, MISO, NCS)`, and `GPIO35–GPIO37` with `SPI3 (MOSI, MISO, NCS)` respectively.
- Enables high-speed serial communication with external peripherals such as sensors or memory devices.
- By default, these pins operate in SPI mode but can be reconfigured as GPIO if required.

Note: Refer to the SPI chapter for detailed information on SPI configuration and usage.

Pin Muxing with General-Purpose Timer (GPTimer)

- `GPIO38–GPIO41` are pin-muxed with `GPTIMER0–GPTIMER3` respectively.
- These pins can be used for event counting, pulse generation, or periodic signal timing.

Note: Refer to the GPTimer chapter for detailed information on GPTimer configuration and usage.

Pin Muxing with JTAG

- `GPIO42–GPIO44` are pin-muxed with `JTAG TDI, TMS, and TDO` respectively.
- Enables debugging and programming functionality.

Note: Refer to the JTAG chapter for detailed information.

6.2.2 ProIO

The **MGS2401 ProIO** feature of GPIO enables **high-speed parallel data transfers through GPIO pins**. Instead of toggling individual GPIOs in software, **ProIO** groups selected pins into fixed-width data buffers, allowing data to be captured or transmitted in parallel with minimal CPU involvement.

Each **ProIO** group operates with its own **FIFO and clocked data interface**, enabling efficient streaming of data between the MCU and external peripherals.

GPIO pins can be organized into the following ProIO groups:

- **Duo** – 2-bit data buffer
- **Tetra** – 4-bit data buffer
- **Octa** – 8-bit data buffer
- **Fusion** – combines the **4-bit (Tetra)** and **8-bit (Octa)** groups to form a **12-bit data interface**

Key Features

- **High-Speed Data Transfer**
  - In **Input mode**, data is sampled from GPIO pins on each configured clock edge and stored in the buffer FIFO.
  - In **Output mode**, data is fetched from the FIFO and driven onto the GPIO pins in synchronization with the clock.
  - Enables **continuous, clock-synchronous data streaming** through GPIO.
  - Supports **DMA-based data transfers**, allowing the FIFO to be serviced automatically without CPU intervention.

- **Integrated FIFO**
  - Each ProIO group includes an internal FIFO to queue data.
  - Reduces software overhead by eliminating the need to service every GPIO transition.
- **Flexible Clocking**
  - Each group includes a **dedicated clock pin**.
  - Supports **internal clock generation with a configurable prescaler** or **external clock input**.
  - Allows easy interfacing with a wide range of peripheral data rates.
- **Configurable Data Groups**
  - Supports **2-bit (Duo), 4-bit (Tetra), 8-bit (Octa), and combined 12-bit (Fusion)** configurations.
- **Selectable Data Access Width**
  - Data can be accessed using **8-bit, 16-bit, or 32-bit transfers**, enabling efficient CPU or DMA interaction.
- **Bidirectional Operation**
  - Groups can operate in:
    * **Input mode (Enqueue)** – capture data from GPIO pins into the FIFO.
    * **Output mode (Dequeue)** – transmit data from the FIFO to GPIO pins.
- **Configurable Clock Edge**
  - Data sampling or transmission can be triggered on either the **rising edge** or **falling edge** of the clock.

6.2.3 Pulse-Width Modulation (PWM)

The device includes 14 PWM instances, each customizable via software. It can be used to control speed of motors, brightness of LEDs, H-bridge motor circuits etc.

- **Prescaler:** These bits select a division factor for the input clock to determine the PWM operating frequency.
- **Duty Cycle:** This register defines the on-time duration (duty cycle) of the PWM waveform as a percentage of the period.
- **Period:** This register sets the overall period of the PWM waveform, determining the frequency.
- **Complementary Output:** It is a functionality that generates an inverted version of the original Pulse Width Modulation (PWM) signal with a programmable dead time. This feature is commonly used for driving complementary MOSFETs in applications like:
  - **Gate Drive Circuits:** Driving the gates of high-side and low-side MOSFETs in a half-bridge configuration for motor control, DC-DC converters, and inverters.
  - **Synchronous Buck-Boost Converters:** Controlling the on/off states of synchronous rectifiers to achieve efficient power conversion.

6.2.4 Serial Peripheral Interface (SPI)

This device has 4 instances of SPI Interface. Each SPI instance can support data transfers upto 35Mbps. The SPI is a synchronous serial I/O port that allows a serial bit stream of programmed length to be shifted into and out of the device at a programmable bit transfer rate. Each SPI module has four external pins - Master in/Slave out(MISO) pin, Master out/Slave in(MOSI) pin, Synchronous clock(SCLK) and Chip Select(CS) pin.

Key Features:

- The SPI peripheral can be configured as either Master or Slave.
- Each instance has interrupts registered with PLIC.

6.2.5 Quad Serial Peripheral Interface (QSPI)

The Quad-SPI (QSPI) module is a high-performance serial communication interface specifically designed for interfacing with external Quad-SPI flash memories. It offers significant advantages over traditional SPI for applications requiring high data throughput and large memory capacity. This device has 2 instances of QSPI interface.

Key Features:

- **Data Transfer:** QSPI utilizes four data lines (I0, I1, I2, I3) compared to the two data lines (MOSI and MISO) used in standard SPI. This quad-channel communication enables significantly faster data transfer rates upto

70Mbps in each data line.

- **Functional Modes:** The QSPI module offers two operational modes for flexible communication with external memory:
  - **Indirect Mode:** Provides complete control over data transfers using dedicated QSPI registers.
  - **Memory-Mapped Mode:** Maps the external memory to the microcontroller's address space, allowing direct access as if it were internal memory. It supports XIP mode, and RAM mode.
- **High-Speed Operation:** Supports Single Data Rate (SDR) mode for optimal data transfer speeds based on application requirements, with a maximum of 70MHz clock frequency, and does data-transfer upto 280Mbps.
- **Programmable Control:** Offers full programmability of opcodes and frame formats for both indirect and memory-mapped modes, ensuring adaptability to various flash memory protocols.
- **Efficient Data Handling:** Integrates FIFOs (First-In-First-Out) for both receive and transmit data paths, streamlining data flow and reducing CPU overhead.
- **Flexible Data Access:** Supports a wide range of data access sizes, including 8, 16, and 32 bits, for compatibility with diverse data types.
- **Comprehensive Interrupt Management:** Generates interrupts on various events, including FIFO threshold reached, timeout conditions, operation completion, and access errors, enabling efficient error handling and system monitoring.
- **Memory Mapped Region:** Supports upto 512 Megabytes storage in the memory-mapped mode for each instance of QSPI. The memory-mapped functional mode supports XIP mode, and RAM mode.

6.2.6 Universal Asynchronous Receiver / Transmitter (UART)

This device has 3 instances of UART interface. Each instance of the UART has interrupt lines that are connected to PLIC.

Key Features:

- The UART supports a wide range of communication speeds upto a baudrate of 1M.
- The UART0 is mapped as the serial console, while subsequent instances are exposed as IO pins.
- To provide more flexibility to the users, the following are software configurable:
  - Supports 1-bit even or odd parity for both transmit and receive modes.
  - Stop bits selection of 1, 1.5, or 2 bits.
  - Character size configuration for character length transmission. It can support 5 to 8-bit characters.
- Has interrupts registered with PLIC for each instance of UART.

6.2.7 Inter-Integrated Circuit interface (I²C)

This device supports has 2 I²C instances that operate at standard mode speed of upto 400 kHz and fast mode speed configurable upto 1MHz.

Key Features:

- The I²C instances supports only master mode operation, and does not work as a slave.
- The I²C instances supports multi-master mode.
- Each I²C instance has an interrupt which is registered with PLIC.
- All the I²C instances support 7-bit addressing mode, with maximum 128 slave devices.

6.2.8 Analog to Digital Converters (ADC)

The device has 1 instance of SAR ADC with 8 channels.

Key Features:

- The ADC has the resolution selectable between 12, 10, 8 and 6 bit.
- It has 5 MSPS Conversion Rate.
- ADC supports 8 channels.

6.2.9 JTAG

The device includes a single **JTAG DTM (Device Transport Module)** that enables JTAG communication with the chip. Through the JTAG interface, it is possible to connect to the processor's debugger, allowing enhanced debugging and development capabilities.

Key Features

- Supports JTAG communication speeds up to **10 MHz**.
- **TRST** (Test Reset) signal is supported.
- **Hardware breakpoints** are supported, enabling easier debugging through external debuggers.

6.2.10 Debugger

This module provides support to the user to check the system's state as required by the user, helping in debugging the system. This module can be accessed via the JTAG connection. This module is compliant with ratified RISC-V Debug Spec v0.13.

Key Features:

- Abstract command and system bus support.
- Can access the core registers, CSRs and memory mapped registers.
- Software breakpoints.

6.2.11 Processor Branch Trace

This module is used to get the program execution trace being a powerfull tool used for debugging user code. This module is compliant with RISC-V E-trace 2.0.0 spec. This module can be used when it is not possible to use a debugger to observe behaviour of a running system as this is intrusive. It is done by recording the discontinuties in the program execution address using the encoder and store the generated packets in a dedicated SRAM which afterwards is read by a host system and decoded to get the program execution trace.

Trace Encoder:

The program execution trace is compressed into smaller packets/payloads using this module.

Key Features:

- The mandatory features mentioned in the RISC V E-trace spec are implemented.
- Additionally, filters are added. These filters can be used to record only necessary parts in a program execution trace. Has support of 3 filters.

Trace RAM sink:

Once the encoder compresses the trace into smaller packets/payloads, they are written and stored in this RAM sink. The size of the RAM sink is 4kB. This trace RAM can then be read via the debugger via which we can extract the packets/payloads and get the trace after decoding.

Key Features:

- Has support for either wrap around or stop filling up the RAM once full.

6.2.12 General-Purpose Timer (GPTimer)

This devices has 4 instances of GPTimer.

Key Features:

- Up, down, up-down counter.
- Simple PWM support.
- Timer capture support.

6.2.13 Watch-Dog Timer (WDTimer)

This device has 1 instance of WDTimer. This module can be used to come out of any system hang.

Key Features:

- Software controlled system reset
- Counter controlled system reset
- Interrupt mode

6.2.14 Platform Level Interrupt Controller (PLIC)

This device receives the interrupts from all the peripherals and notifies the system for an interrupt.

Key Features:

- Interrupt from 63 sources are connected.
- Interrupt priority value upto 7.
- A threshold register to service interrupts above a required priority value.

6.2.15 Direct Memory Access (DMA)

The Direct Memory Access (DMA) controller enables high-speed data transfers between memory and peripherals without continuous CPU intervention.

Key Features:

- Provides **8 independent channels**, which are serviced **sequentially** based on their assigned priority levels.
- Supports **memory-to-memory**, **peripheral-to-memory**, **peripheral-to-peripheral** and **memory-to-peripheral** transfer modes.
- Each channel supports data widths of **8-bit**, **16-bit**, **32-bit**, or **64-bit**.
- Each channel supports **four priority levels (0–3)** .

6.2.16 Pin Multiplexing (PINMUX)

Pinmux (Pin Multiplexing) is a mechanism that allows a single physical pin to support multiple alternate functions.

Key Features

- Allows a **single pin to support multiple alternate peripheral functions**.
- Enables configuration of pins for interfaces such as **GPIO, UART, SPI, PWM, JTAG**, etc.
- Only **one function can be active on a pin at a time** to avoid peripheral conflicts.

Pinmux Register Map

Register Name	Offset (Hex)	Function when clear	Function when set
MUX0	0x0000	GPIO0	PWM0
MUX1	0x0004	GPIO1	PWM1
MUX2	0x0008	GPIO2	PWM2
MUX3	0x000C	GPIO3	PWM3
MUX4	0x0010	GPIO4	PWM4
MUX5	0x0014	GPIO5	PWM5
MUX6	0x0018	GPIO6	PWM6
MUX7	0x001C	GPIO7	PWM7
MUX8	0x0020	GPIO17	PWM8
MUX9	0x0024	GPIO18	PWM9
MUX10	0x0028	GPIO19	PWM10

Register Name	Offset (Hex)	Function when clear	Function when set
MUX11	0x002C	GPIO20	PWM11
MUX12	0x0030	GPIO21	PWM12
MUX13	0x0034	GPIO22	PWM13
MUX14	0x0038	SPI2_MOSI	GPIO32
MUX15	0x003C	SPI2_MISO	GPIO33
MUX16	0x0040	SPI2_NCS	GPIO34
MUX17	0x0044	SPI3_MOSI	GPIO35
MUX18	0x0048	SPI3_MISO	GPIO36
MUX19	0x004C	SPI3_NCS	GPIO37
MUX20	0x0050	GPIO8	UART3_TX
MUX21	0x0054	GPIO9	UART3_RX
MUX22	0x0058	GPIO11	UART4_TX
MUX23	0x005C	GPIO15	UART4_RX
MUX24	0x0060	GPTIMER0	GPIO38
MUX25	0x0064	GPTIMER1	GPIO39
MUX26	0x0068	GPTIMER2	GPIO40
MUX27	0x006C	GPTIMER3	GPIO41
MUX28	0x0070	JTAG_TDI	GPIO42
MUX29	0x0074	JTAG_TMS	GPIO43
MUX30	0x0078	JTAG_TDO	GPIO44

Table 3: Pin Functions

6.3 Security accelerators

This microcontroller integrates a powerful suite of security accelerators designed to safeguard your applications and data. These accelerators offload computationally intensive cryptographic operations from the main CPU, enabling:

- **Reduced Power Consumption:** By offloading encryption and decryption tasks to dedicated hardware, power usage associated with these security operations can be minimized, extending battery life in portable devices.
- **Enhanced Security:** The dedicated security accelerators free up valuable CPU resources, allowing the main processor to concentrate on core application functionalities while ensuring robust cryptographic operations in the background.

The following industry-standard algorithms are supported in hardware.

6.3.1 RSA

This versatile public-key cryptography algorithm is widely used for digital signatures and secure key exchange. Hardware acceleration significantly improves the performance of RSA encryption and decryption operations, especially for larger key sizes like 2048 bits, which offer a high level of security.

The on-board RSA accelerator supports 2048 bit keys.

6.3.2 AES

This widely adopted symmetric key algorithm is a cornerstone of modern cryptography. AES hardware acceleration empowers you to encrypt and decrypt data efficiently, protecting sensitive information at rest and in transit. This device has support for AES 128,192,256 with Cipher Block Chaining mode, Cipher FeedBack mode, Output FeedBack mode and Counter mode.

6.3.3 SHA-2

This cryptographic hash function generates a unique and fixed-size fingerprint from a data stream. Hardware acceleration for SHA256 enables efficient message integrity verification and digital signature validation, ensuring data authenticity and tamper detection.

6.3.4 One-Time Programmable Memory (OTP Memory)

The device has 32 Kbit of OTP that provides secure storage for sensitive data like cryptographic keys. It is also used for Secure-Boot of MGS2401. This tamper-resistant memory ensures the confidentiality and integrity of your sensitive information.

6.3.5 True Random Number Generator (TRNG)

The device has a single instance of NIST SP800-90C compliant True Random Number Generator. This hardware module generates unpredictable numbers essential for cryptographic operations, strengthening the overall security posture of your system.

Key Features:

- Background noise collection to speed reseeding operations.
- Entropy Dispatch Unit (EDU) to provide multi-master support, serial entropy streams, and ESM nonce port.
- Internal random seeding operation.
- 128-bit random number generation.
- Start-up, continuous and on-demand health tests.
- Compliant with NIST SP800-90A/B/C and BSI AIS 20/31.
- 128-bit or 256-bit of security strength.
- Ring oscillator-based Bit Generator blocks with wide system clock rate dynamic range.

6.4 Pin Functions

Signal	Function	I/O	Description
PLL_VREF	Analog Signal	Input	External voltage reference for PLL. Connect it to VDD_IO.
ADC_DISLVL	Analog Signal	Input	Analog input output.
CLK	Clock	Input	External reference clock (20MHz).
SPIx_SCLK	SPI	Output	Provides the clock signal that synchronizes data transfer between the master and slave devices.
SPIx_NCS	SPI	Output	Used by the master to select a specific slave device. A low signal on this pin selects the slave.
SPIx_MISO	SPI	Input	Carries data from the slave device to the SPI master.
SPIx_MOSI	SPI	Output	Carries data from the SPI master to the slave device.

Signal	Function	I/O	Description
I2Cx_SDA	I2C	Open-Drain	This pin acts as the input and output during data transfer w.r.t I2Cx_SCL.
I2Cx_SCL	I2C	Open-Drain	Provides I2C clock signal that synchronizes data transfer between the slave device.
ADCx	ADC	Input	Single ended input with 8/10/12 bit resolution.
GPIOx/PWMx	GPIO/PWM	Inout	General purpose Input and output pinmuxed with PWM.
GPIOx	GPIO	Inout	General purpose Input and output.
TIMER	GPTIMER	Inout	Timer Interrupt.
TDI	JTAG	Input	Test Data Input.
TDO	JTAG	Output	Test Data Output pin that carries data out from the JTAG interface of the device being tested.
TMS	JTAG	Input	Controls the operational state of the JTAG interface by applying a specific sequence of logic levels.
TCK	JTAG	Input	Provides the clock signal that synchronizes data transfer on the TDI and TDO lines.
TRST	JTAG	Input	Pin can be tied to high with Vref.
QSPIx_NCS	QSPI	Input	QSPI chip select input.
QSPIx_CLK	QSPI	Output	QSPI serial clock pin provides the timing for serial input and output operations.
QSPIx_IO[0]	QSPI	Inout	In standard SPI used as only one data line (MISO).
QSPIx_IO[1]	QSPI	Inout	In standard SPI used as only one data line (MOSI).
QSPIx_IO[2]	QSPI	Inout	Works alongside IO0 and IO1 to achieve quad data transfer.
QSPIx_IO[3]	QSPI	Inout	Works alongside IO0, IO1 and IO2 to achieve quad data transfer.
UARTx_TX	UART	Output	Transmit data.
UARTx_RX	UART	Input	Receive data.

Note: The ‘x’ present in QSPIx, SPIx, GPIOx, PWMx, I2Cx, UARTx and ADCx specifies the instance number for each peripheral. Can be used as, QSPI0, SPI1, UART2 etc. I2Cx works based on open drain/emulator configuration.

7 Boot Configuration

Mindgrove Silicon's MGS2401 provides Secure-Boot capability. The boot configuration is stored in the on-chip Boot-ROM.

7.1 Boot Modes Supported

1. Secure-Boot with QSPI0/QSPI1.
2. Normal-Boot with QSPI0/QSPI1.
3. Parking Loop if QSPI0/QSPI1 is not available.

7.2 Prerequisites for Boot

For successful booting of the software application, in modes 1 and 2, the following are expected to be present.

1. QSPI Flash connected to QSPI0 or QSPI1 interface, programmed with valid software application. The flash must be capable of supporting XIP (eXecute In Place) mode. It is requested because, the QSPI0 or QSPI1 will change its mode to XIP, in which the programs starts executing from the flash memory, rather than copying it into the RAM and running.
2. UART0 is set as the Serial Output by default, and cannot be changed by the user. The baudrate to be set in the Serial-Terminal to view the output should be 115200.

7.3 Boot Process

Upon powering on or resetting, the MGS2401 begins by reading OTP memory to check the `JTAG_LOCK` bit, locking the JTAG interface if set, or leaving it open for development if not.

The system then probes QSPI0 for a valid SFDP response, falling back to QSPI1 if needed. If neither interface yields a valid flash device, the system sets `BOOT_STATUS: NO_FLASH` and halts.

Once a flash source is confirmed, the bootloader checks for a custom QSPI configuration header. It applies custom XIP settings to flash if custom QSPI configuration header is found, or falls back to default XIP settings otherwise.

It then reads the application image size. If the size exceeds 16 MB, the system halts with `BOOT_STATUS: INVALID APP LEN`.

A validity check on the application entry point is then performed, which triggers `BOOT_STATUS: NO_APPLN` and a halt if an invalid pattern is detected.

If the application headers are valid, the bootloader consults OTP to determine whether secure boot is enabled. If not, the application executes directly.

If secure boot is enabled, the bootloader reads public key data from OTP, blocking debug access. If no key or an invalid key is found in OTP, the core stalls with `ERR_CODE: NO PUB KEY` or `ERR_CODE: INVALID PUB KEY`.

It then verifies PKCS #1 v1.5 padding in the decrypted signature and compares the runtime SHA hash against the signed hash. On failure, the system halts with `ERR_CODE: RSA_PKCS_DECRYPT` or `ERR_CODE: SHA_MISMATCH`, respectively.

A fully successful secure boot proceeds to application execution.

Should an exception occur at any point during execution, the trap handler logs the `mcause` and `mepc` registers and halts in a while loop.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Description	Min	Typ	Max
Supply Voltage	VDD_CORE	Maximum voltage that can be applied to the power supply pins.	0.81V	0.9V	0.99V
Input/Output Voltage	VDD_IO	Maximum voltage that can be applied to input/output pins.	1.62V	1.8V	1.98V
Reference power supply voltage	PLL_VREF	External voltage reference for PLL.	0.81V	0.9V	0.99V
Analog power supply voltage	AVDD_PLL	Analog 0.9 V power supply for PLL.	0.81V	0.9V	0.99V
Analog power ground voltage	AGND_PLL	Dedicated Analog ground for PLL 0.9 V supply.	0V	0V	0V
High-Voltage Analog Power Supply	AVDDHV_PLL	Dedicated Analog 1.8 V power supply for PLL.	1.62V	1.8V	1.98V
High-Voltage Analog Ground	AGNDHV_PLL	Dedicated Analog ground for PLL 1.8 V supply.	0V	0V	0V
Load capacitance	(C)	Capacitance.	5pF	—	25pF

Table 5: Absolute Maximum Ratings

8.2 Operating Conditions

TBD

8.3 Power Consumption

TBD

8.4 Thermal Characteristics

Paramater	Symbol	Description	Min	Typ	Max
Operating Temperature	(Tj)	Temperature range for safe device operation.	-40°C	25°C	+85°C

Table 6: Thermal Characteristics

8.5 Timing

TBD

9 PCB Guidelines

- All capacitors for the supply VDD_CORE, VDD_IO, AVDDHV_ADC, AVDD_PLL, AVDDHV_PLL must be as close as possible to the respective pins. The smallest capacitors must be the closest to the package pins.

9.1 PLL

- Place capacitors between (typically 0.1uF ceramic) AVDD_PLL to gnd. Power pins should be close to capacitors.
- External supply noise should be kept to a minimum, and special care should be taken to avoid low frequency (<1MHz) ripple noise content, for example originated from low frequency power management events or DC-DC conversion.
- The clock trace should be well isolated from other noisy PCB traces.
- Prioritize placing the crystal oscillator in close proximity to the relevant input and output pins.
- Avoid placing clock lines and switching signal lines near crystals and their connections.

9.2 ADC

- Place 0.01- F bypass capacitor between AVDDHV_ADC to gnd.
- All capacitors for ADC0-7, ADC_VREF must be as close as possible to the respective package pins.
- ADC0-7 lines must be shielded.
- To enable/diable ADC, it can be tied to low/high in the PCB respectively.

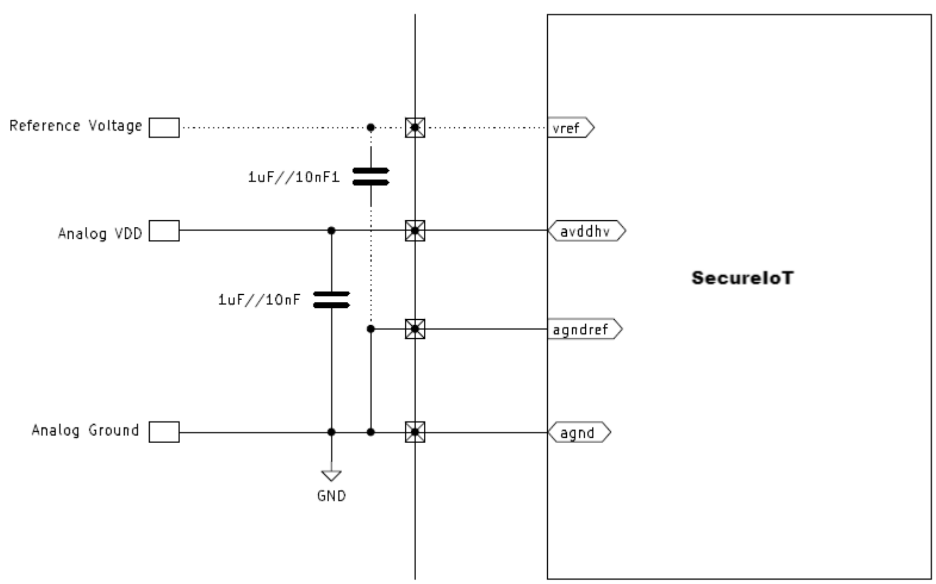

Figure 3: ADC Decoupling Schematic

9.3 I2C

- Pull-up resistors are used to keep the SDA and SCL lines at a high voltage level when they are not being driven by the devices.

- I2C bus loads should be kept to a minimum to reduce the number of devices. Signal degradation and communication problems may occur if too many devices are connected to the bus.
- Avoid routing high speed signals near the SDA and SCL traces.

9.4 QSPI

- Place decoupling capacitors (typically 0.1uF ceramic) close to the VDD_IO and ground pins of the QSPI device.
- Apply impedance control of 50 Ohms on the clock and data interfaces.
- Place series termination 39E to all qspi digital pins and clock pins.
- Place the clock line (QSPI_CLK) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data traces.
- Place data signals at least one trace width away from any copper plane.
- Keep all QSPI traces (clock, data lines, chip select) as short as possible, especially between the controller and the QSPI device.

9.5 JTAG

- Keep JTAG traces (TCK, TMS, TDI, TDO, TRST*) as short as possible, especially between the JTAG connector and the first JTAG-enabled device. This reduces signal delay and minimizes noise pickup.
- Matched lengths between the JTAG header and each device's JTAG pins. This ensures signals arrive simultaneously for proper operation.
- Provide a dedicated ground plane for JTAG signals to minimize noise. Connect this plane to the system ground at a single point to avoid ground loops.

10 Software and Tools

10.1 SDK

The software development kit (SDK) provides the tools required for baremetal software development. The SDK includes the baremetal library which contains the peripheral drivers, and example programs for peripherals like UART, GPIO, ProIO, I2C, SPI, QSPI, PWM etc., along with some application drivers such as LCD, RTC etc. The SDK also includes the drivers and example programs for hardware based crypto-accelerators like AES, SHA, RSA etc.

10.1.1 Tools Required

1. RISC-V GNU Toolchain - for compiling and debugging.
2. Open On Chip Debugger - for JTAG based debugging.
3. Serial Terminal (e.g., GTKTerm, puTTY) - for viewing outputs.

Note: The SDK can be accessed upon request.

10.2 IDEs

The supported IDEs for software development include the following:

- Microsoft Visual Studio Code,
- Eclipse

The provided code examples can be run using these IDEs.

10.3 RTOSs

Currently, the following RTOSs have been tested with MGS2401:

- FreeRTOS
- Zephyr OS
- NuttX

For the above mentioned Real-Time Operating Systems, all the peripheral drivers are included.

11 Package Information

11.1 WBGA144

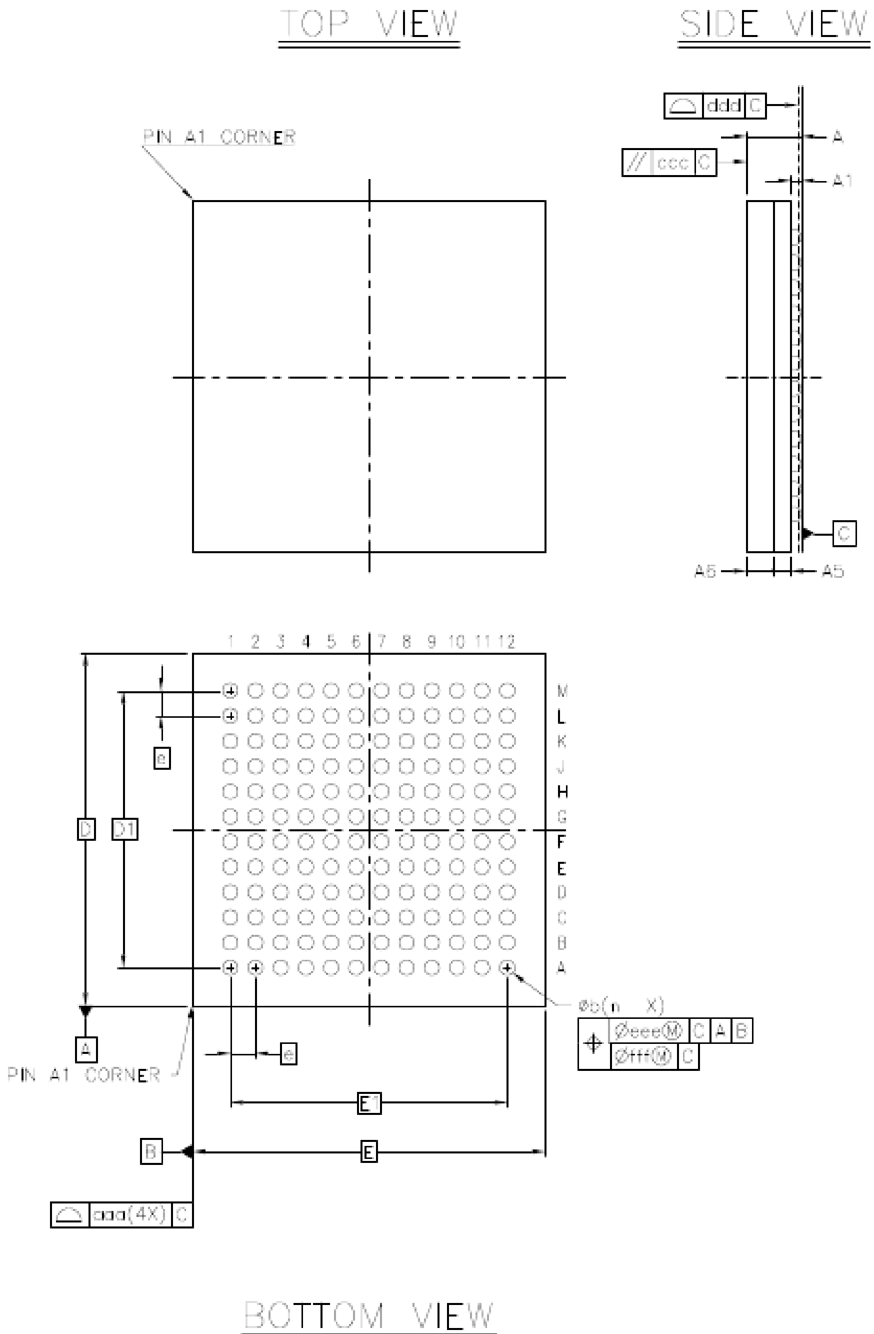

Figure 4: WBGA144 Package

Package / Item	Sub	Symbol	MIN	NOM	MAX
Package				TFBGA	
Body Size	X	E	6.900	7.000	7.100
	Y	D	6.900	7.000	7.100
Ball Pitch		e		0.500	
Total Thickness		A	1.136	1.212	1.288
Mold Cap Thickness		A6		0.650	Ref.
Substrate Thickness		A5		0.352	Ref.
Ball Diameter				0.300	
Stand Off		A1	0.160	0.210	0.260
Ball Width		b	0.270	0.320	0.370
Package Edge Tolerance		aaa		0.100	
Mold Parallelism		ccc		0.100	
Coplanarity		ddd		0.080	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.080	
Ball Count		n		144	
Edge Ball Center to Center	X	E1		5.500	
	Y	D1		5.500	

Table 7: WBGA144 Package Details

12 Glossary and references

- RISC-V International: https://riscv.org/
- SHAKTI Processor: https://shakti.org.in
- RISC-V ISA Specifications:
  - Unprivileged Specification
  - Privileged Specification
- RISC-V Non-ISA Specifications:
  - Efficient Trace
  - RISC-V ABIs
  - RISC-V Debug
  - RISC-V Platform Level Interrupt Controller
  - RISC-V Supervisor Binary Interface
- OCSRAM: On-chip SRAM
- OTP Memory: One-Time Programmable Memory

13 Revision History

Rev. No	Date	Description	Modified by	Approved by
1.0	03-06-2024	Initial revision for Secure IoT MPW	M. Kapil Shyam	Shashwath T.R.
1.1	09-09-2024	Updated PCB Layout Guidelines	Swaathi S	Shashwath T.R.
1.2	27-12-2024	Updated Part code ordering info	Mouna Krishna	Shashwath T.R.
2.0	27-03-2026	Updated Boot Sequence, ProIO details, Package details	Deeptha G	M. Kapil Shyam
2.1	15-07-2026	Updated Pin diagrams for QFN and BGA	Deeptha G	M. Kapil Shyam

Table 8: Revision history